art, the growth of an oxide having a thickness of about 2000 Å will typically consume about 0.1 μm of semiconductor material. Accordingly, the initial widths of the mesas **17** should be selected so that at the end of processing the widths are at the desired value of about 0.5 μm.

Referring now to FIGS. **2E–2K**, a conformal N-type first polycrystalline silicon region **26** is then deposited and etched until it is recessed in the trench to a depth just below the second P-N junction (**J2**). An oxide etching step is then performed to remove the first electrically insulating region **24** from the portions of the sidewalls **20***a* which extend adjacent the etched source and channel regions **18** and **16**, as illustrated best by FIG. **2F**. Referring now to FIG. **2G**, a second electrically insulating region **28** (e.g., SiO_2) having a second thickness less than about 1000 Å and more preferably about 500 Å, is then formed on the trench sidewalls **20***a*, adjacent the etched source and channel regions. The second electrically insulating region **28** is then selectively etched from the top of the first polycrystalline silicon region **26** but not the sidewalls **20***a*, using a reactive ion etching (RIE) technique. Referring now to FIG. **2H**, a conformal second polycrystalline silicon region **30** is then deposited on the first polycrystalline region **26** and the second electrically insulating region **28**. The second polycrystalline silicon region **30** is then etched until it is recessed in the trench to a depth just below the first face **15***a*.

A third electrically insulating region **32** is then formed on the etched second polycrystalline silicon region **30** by oxidizing the second polycrystalline silicon region **30**, as illustrated by FIG. **2I**. The stress relief oxide layer **22***a* and the oxide barrier layer **22***b* (e.g., Si_3N_4) are then etched to expose the source region **18** and channel region **16** at the first face **15***a*, as illustrated by FIG. **2J**. A source metal contact layer **34** is then deposited on the first face **15***a* and a drain metal contact layer **36** is deposited on an opposing second face **151***b* to form ohmic contacts to the source and channel regions (**18** and **16**) and drain region **14**, respectively, as illustrated by FIG. **2K**. As described above, the source metal contact layer **34** will also ohmically contact the portions of the channel region **16** which extend to the first face **15** in the third dimension (not shown).

Referring now to FIG. **3**, a unit cell **100** of a silicon field effect transistor according to a preferred embodiment of the present invention and a graph of the doping profiles of the layers therein are illustrated. The unit cell **100** has a width "W_c" of 1 μm and comprises a highly doped drain layer **114** of first conductivity type (e.g., N+), a drift layer **112** of first conductivity type having a linearly graded doping concentration, a relatively thin channel layer **116** of second conductivity type (e.g., P-type) and a highly doped source layer **118** of first conductivity type (e.g., N+), arranged as illustrated. In particular, the drift layer **112** is preferably formed by epitaxially growing an N-type in-situ doped monocrystalline silicon layer having a thickness of 4 μm on an N-type drain layer **114** (e.g., substrate) having a thickness of 100 μm and a doping concentration of greater than 1×10^{18} cm^{-3} (e.g. 1×10^{19} cm^{-3}). As illustrated, the drift layer **112** has a linearly graded doping concentration therein with a maximum concentration of 3×10^{17} cm^{-3} at the N+/N junction with the drain layer **114** and a minimum concentration of 1×10^{16} cm^{-3}, beginning at a distance 3 μm from the N+/N junction and continuing to the first face **15***a*.

The channel layer **116** is preferably formed by implanting a P-type dopant such as boron into the drift layer **112** at an energy of 100 kEV and a dose of 1×10^{14} cm^{-2}. The P-type dopant is then diffused to a depth of 0.5 μm into the drift layer **112**. An N-type dopant such as arsenic is then performed at an energy of 50 kEV and a dose of 1×10^{15} cm^{-2}. The N-type and P-type dopants are then diffused to a depth of 0.5 μm and 1.0 μm, respectively, to form a vertical stack containing the drain, drift, channel and source layers.

A stripe-shaped trench having a pair of opposing sidewalls **120***a* which extend in a third dimension (not shown) and a bottom **120***b* is then formed in the stack. For a unit cell **100** having a width W_c of 1 μm, the trench is preferably formed to have a width "W_t" of 0.5 μm at the end of processing. An insulated gate electrode comprising a gate insulating region **124** and an electrically conductive gate **126** (e.g., polysilicon) are then formed in the trench. According to the preferred embodiment, the portion of the insulating region **124** extending adjacent the trench bottom **120***b* and the drift layer **112** has a thickness "T_1" of about 2000 Å to inhibit the occurrence of high electric field crowding at the bottom corners of the trench and to provide a substantially uniform potential gradient along the trench sidewalls **120***a*. Although not wishing to be bound by any theory, the uniformity of the potential gradient along the trench sidewalls can also be enhanced by making the product of the doping concentration in the drift layer **112** at **J3** (e.g., 3×10^{17} cm^{-3}) and the width of the mesa between adjacent trenches (e.g., 0.5 μm) within the range of 1×10^{13}–2×10^{13} cm^{-2} and by making the produce of the doping concentration in the drift layer **112** at **J2** and the width of the mesa within the range of 1×10^{11}–2×10^{12} cm^{-2}. The portion of the insulating region **124** extending adjacent the channel layer **116** and the source layer **118** preferably has a thickness "T_2" of about 500 Å to maintain the threshold voltage of the device at about 2–3 volts. Simulations of the unit cell **100** at a gate bias of 15 Volts confirm that a vertical silicon field effect transistor having a maximum blocking voltage capability of 60 Volts and a specific on-resistance ($R_{sp,on}$) of 40 $\mu\Omega cm^2$, which is four (4) times smaller than the ideal specific on-resistance of 170 $\mu\Omega cm^2$ for a 60 volt power UMOSFET, can be achieved. Accordingly, it is not necessary to form a uniformly thick 2000 Å gate oxide to achieve 60 volt blocking capability with a resulting increase in threshold voltage and specific on-resistance.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A field effect transistor, comprising:

a semiconductor substrate having first and second opposing faces;

a source region of first conductivity type in said substrate, adjacent the first face;

a drain region of first conductivity type in said substrate, adjacent the second face;

a drift region of first conductivity type in said substrate, said drift region extending between said drain region and said source region and having a graded first conductivity type doping concentration therein which decreases in a direction from said drain region to said source region;

a channel region of second conductivity type in said substrate, said channel region extending between said source region and said drift region and forming first and second P-N junctions therewith, respectively;

a trench in said substrate at the first face, said trench having a sidewall extending adjacent said drift region and said channel region; and